AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions, and listings of claims in the applicants.

Listing of Claims

1. (Currently Amended) A system for resequencing per flow data packets received by at least one destination egress adapter comprising:

a plurality of output registers with each register dynamically assigned to store received data packets from one of a plurality of flows;

~~means (271) for allocating a temporary storage location in a packet buffer to each received data packets;~~

a packet buffer;

means for allocating a temporary storage location in the packet buffer for each received data packet;

means ~~(510,550),~~ using predefined parameters, for pointing to an output register ~~(540)~~ previously assigned to receive data packets from a corresponding flow; and

means ~~(270 271)~~coupled to the allocati~~o~~ng means and to the

pointing means for determining if each received data packet is the next in sequence of the corresponding flow, by comparing the packet sequence number (PSN) of said each received data packet to the last packet sequence number (PSNc,PSNh) used by the pointed output register.

2. (Currently amended)The system of claim 1 wherein the means for pointing to an output register comprise a first Content Addressable Memory ~~(510)~~ wherein each entry ~~(512)~~ includes a search field ~~(515)~~ having a source identifier, a routing index and a priority level, and an associated identifier field including a Cross Reference Index (520) to point to a previously assigned output register among a plurality of output registers ~~(500)~~.

3. (Currently amended)The system of claim 2 wherein the identifier field further contains an activity identifier ~~(521)~~ to indicate when a previously assigned output register is no longer active, and a packet sequence number ~~(522)~~ equal to the last packet sequence number received for the corresponding flow.

4. (Currently Amended)The system of claim 2 wherein the means for pointing further comprise means ~~(550)~~ for providing a new output register to each new flow of data packets.

5. (Currently amended)The system of claim 2 wherein the first Content Addressable Memory further comprises means ~~(514,523)~~ for preventing over filling of said first Content Addressable Memory.

6. (Currently Amended))The system of claim~~s 1 or~~ 2 further comprising a second Content Addressable Memory ~~(400)~~ wherein each entry including a source identifier ~~(415)~~ a routing index ~~(420),~~ a priority level ~~(425)~~ and the packet sequence number ~~(430)~~ of each stored data packet, and an associated identifier field ~~(435)~~ to give a packet buffer identifier (ID) that identifies the storage location allocated to each received data packet.

7.(Currently Amended)The system of claim 1 wherein each of the output registers~~(540)~~ further comprises:

a packet sequence number ~~(501)~~ and a packet buffer identifier ~~(502)~~ for an in-process data packet; and

a valid-bit latch ~~(505)~~ to set an active/not active status that indicates if the in-process data packet is already output.

8. (Currently Amended)) The system of claim 7 wherein the output register further comprises a counter~~(503)~~ to maintain a value for, each flow, the number of data packets stored in the packet buffer waiting to be transmitted.

9. (Currently amended) The system of claim 7 further comprising scheduling means ~~(280)~~ coupled to the determination means for selecting one of the in-process data packets to be output.

10. (Currently amended)~~1.~~ A system for resequencing per flow data packets received by at least one destination egress adapter comprising:

a plurality of output registers with each register dynamically assigned to store received data packets from one of a plurality of flows, ~~7.The system of claim 1~~ wherein each of the output registers~~(540)~~ further comprises:

a packet sequence number ~~(501)~~ and a packet buffer identifier ~~(502)~~ for an in-process data packet; and

a valid-bit latch ~~(505)~~ to set an active/not active status that indicates if the in-process data packet is already output;

means ~~(271)~~ for allocating a temporary storage location in a packet buffer to each received data packet~~s~~;

means ~~(510,550),~~ using predefined parameters, for pointing to an output register (540) previously assigned to receive data packets from a corresponding flow; and

means ~~(270 271)~~coupled to the allocati~~o~~ng means and to the pointing means for determining if each received data packet is the next in sequence of the corresponding flow, by comparing the packet sequence number (PSN) of said each received data packet to the last packet sequence number (PSNc,PSNh) used by the pointed output register ~~9. The system of claim 7 further comprising~~ and scheduling means ~~(280)~~ coupled to the determination means for selecting one of the in-process data packets to be output, ~~The system of claim 9~~ wherein the scheduling means is coupled to each of the valid-bit latches to select one valid-bit latch having an active status.

11. (Currently Amended)The system of claims 1 or 2 wherein the means ~~(265)~~ for allocating comprise a free buffer list ~~(470)~~ to allocate a free temporary storage location (ID) to each received data packet. ~~(460)~~

12. Original) The system of claims 1 or 2 wherein the data packets comprise unicast and multicast data packets.

13. (Currently amended) The system of claim 1 further including at least one ingress adapter comprising counting means ~~(210,360,385)~~ for sequentially numbering data packets of a same flow.

14. (Currently Amended)The system of claim 13 wherein the ingress adapter further comprises means ~~(205)~~ for load balancing the data packets over a plurality of independent switching planes.

15. (Currently amended) ~~1.~~ A system for resequencing per flow data packets received by at least one destination egress adapter comprising:

a plurality of output registers with each register dynamically assigned to store received data packets from one of a plurality of flows;

means ~~(271)~~ for allocating a temporary storage location in a packet buffer to each received data packet~~s~~;

means ~~(510,550),~~ using predefined parameters, for pointing to an output register ~~(540)~~ previously assigned to receive data packets from a corresponding flow; and

means ~~(270 271)~~coupled to the allocati~~o~~ng means and to the pointing means for determining if each received data packet is the next in sequence of the corresponding flow, by comparing the packet sequence number (PSN) of said each received data packet to the last packet sequence number (PSNc,PSNh) used by the pointed output register and ~~13. The system of claim 1 further including~~ at least one ingress adapter comprising counting means ~~(210,360,385)~~ for sequentially numbering data packets of a same flow; ~~The system of claim 14 wherein the~~ ~~at least one ingress adapter further comprising 14. The system~~ ~~of claim 13 wherein the ingress adapter further comprises~~ means ~~(205)~~ for load balancing the data packets over a plurality of independent switching planes; and

means ~~(220)~~ for scheduling the switching of the data packets over the plurality of independent switching planes.

16. (Currently amended) A method for resequencing per flow ~~the~~ data packets received by at least one destination egress adapter comprising:

~~(605)~~ allocating a temporary storage location in a packet buffer to each received data packet;

providing a plurality of output registers with each register dynamically assigned to store received data packets from one of a plurality of flows;

~~(610)~~ extracting predefined parameters from said each received data packets;

using the predefined parameters to search a memory and identifying a cross reference index;

using the Cross Reference Index associated with each received data packet to point ~~(625)~~ to a respective output register previously assigned to the corresponding flow of each received data packet; and

comparing ~~(640)~~ ~~the~~ a packet sequence number of each received data packet to a packet sequence number stored in the respective pointed output register to determine if said each received data packet is the next in sequence.

17. (Currently amended) The method of claim 16 further comprising:

assigning ~~(660)~~ a new output register and a new Cross Reference Index if no associated Cross Reference Index is found ~~(617)~~ for a received data packet; and

storing ~~(690)~~ in the new output register the packet sequence number (PSN) of said received data packet.

18. (Original) The method of claim 16 further comprising checking if the assigned output register is active.

19. (currently amended) The method of claim 18 further comprising:

assigning ~~(650)~~ a new output register if the assigned output register is found inactive;

comparing ~~(655)~~ the packet sequence number of the received data packet to the last packet sequence number used by the inactive assigned output register; and

storing ~~(690)~~ in the new output register the packet sequence number (PSN) of said received data packet if it is the next in sequence, otherwise

storing ~~(670)~~ in the new output register the last packet sequence number (PSNh) used by the inactive assigned output register.

20. (Currently amended) The method of claim~~s~~ 16 or17 further comprising releasing ~~the~~ an unused Cross Reference Index after a predetermined time interval.

21. (Currently amended) ~~16.~~ A method for resequencing per flow the data packets received by at least one destination egress adapter comprising:

~~(605)~~ allocating a temporary storage location in a packet buffer to each received data packet;

~~(610)~~ extracting predefined parameters from said each received data packets;

using the predefined parameters to search a memory and identifying a cross reference index;

using the Cross Reference Index associated with each received data packet to point ~~(625)~~ to a respective output register previously assigned to the corresponding flow of each received data packet; and

comparing ~~(640)~~ ~~the~~ a packet sequence number of each received data packet to a packet sequence number stored in the respective pointed output register to determine if said each received data packet is the next in sequence; ~~.~~

~~18. (Original) The method of claim 16 further comprising~~

checking if the assigned output register is active; ~~.~~

~~19. (currently amended) The method of claim 18 further comprising:~~

assigning ~~(650)~~ a new output register if the assigned output register is found inactive;

comparing ~~(655)~~ the packet sequence number of the received data packet to the last packet sequence number used by the inactive assigned output register; ~~and~~

storing ~~(690)~~ in the new output register the packet sequence number (PSN) of said received data packet if it is the next in sequence, otherwise

storing ~~(670)~~ in the new output register the last packet sequence number (PSNh) used by the inactive assigned output register; ~~.~~

~~The method of claim 19 wherein the assigned output registers further comprise~~ and a packet buffer identifier that identifies the storage location (ID) allocated to each received data packet.

22. (Currently amended) The method of claims 16 or 17 further comprising writing in a Content Addressable Memory, ~~the~~ a source identifier, ~~the~~ a priority level and the packet sequence number of each received data packet that is not the next in sequence, the write address being identified by the storage location allocated to said each received da ta packet.

23. (Currently amended) The system of claims 1 ~~or 16~~ wherein the predefined parameters include Priority Level (PTY), Routing Index (RI) and Source Identifier.

24. (Original) A method comprising:

providing a plurality of registers with each register associated with a flow:

providing a cross reference table with each entry associated with a register within said plurality of registers;

receiving a packet;

searching the cross reference table with parameters selected from the packet;

if a match is found, correlating at least one parameter identified in a register associated with said matching entry with parameter in the packet to determine sequence of said packet relative to a packet identified in said associated register.

25. (Previously Presented) The method of claim 24 further including if a match is not found making a new entry for said packet in said cross reference table and associating a register from said plurality of registers with said packet and flow to which the packet belongs.

26. (Previously Presented) The method of claim 24 further including if the packet is in sequence with packet identified in said associated register setting a valid bit to post request for service to egress scheduler.

27. (Previously Presented)The method of claim 24 further including if the packet is out of sequence relative to the packet identified within said associated register reset a valid bit indicating no request is posted to egress scheduler.

28. (Currently Amended) A ~~program product comprising~~:

~~a~~ computer readable medium ~~encoded~~ embodied with a computer readable code, said computer readable code including a first instruction module with instructions to examine a packet and extract a set of predefined parameters therefrom;

a second instruction module with instructions that use the extracted predefined parameters to search an index table having a plurality of entries with each entry associated with a different register; and

a third instruction module having instructions that correlate parameters in said packet with parameters stored in an associated register to determine sequence of said packet to packet identified in said register, if a match is found between the extracted predefined parameter and an entry in said index table.

29. (Currently amended) The ~~program product~~ computer readable medium of claim 28 further including a fourth instruction module including instructions for adding an entry for said packet to the index table if a match is not found.

30. (Previously Presented) An apparatus comprising:

a plurality of switching planes;

a buffer for storing packets transported through said switching ~~panes~~ planes;

a system for ensuring packets are in predefined sequence said system including a register stack wherein each register is associated with a different flow of a multi flow system;

a cross reference index table having a plurality of entries with each entry associated with a different register in said register stack; and

a controller that selects parameters from a received packet to search the index table and determine sequence of said packet relative to a packet identified in a register associated with a match entry.